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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,173	01/14/2004	Nian Yang	AMD-AF01210	4822

7590 01/21/2005
WAGNER, MURABITO & HAO LLP
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EXAMINER

WILSON, SCOTT R

ART UNIT PAPER NUMBER

2826

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/758,173	Applicant(s) YANG ET AL.	
	Examiner Scott R. Wilson	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-9, 14-16 and 18-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-9, 14-16 and 18-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 6-9, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al..

As to claim 6, Huang et al., Figures 3 and 4, discloses a semiconductor structure comprising a pad area (200), an electrostatic discharge protective device disposed below said pad area, said electrostatic discharge protective device comprising a transistor (218) and a resistance, embodied as the conductive structure formed below the pad (200) and above the transistor (218), wherein said pad area comprises: a substrate (150), a first layer of metal (208) disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal, and a second layer of metal (204) disposed above said first layer of metal, a layer of dielectric (230) disposed between said first metal layer and said second metal layer, and a via (202) disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, and wherein said via comprises a plurality of individual vias and said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

As to claim 7, Huang et al. discloses (col. 4, lines 35-39) that the conductive structure comprised of layers (204, 208, 212) and vias (202, 206, 210), as well as lines (226, 222, 212a) and (224, 220, 214) may all be formed from polysilicon, which has a known resistance. The fabrication of this structure determines the amount of polysilicon used, and therefore fixes the overall resistance.

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As to claim 8, the structure of Huang et al., Figure 4, would have more resistance if fewer vias were formed, and less resistance if more vias were formed. See (col. 4, lines 45-50).

As to claim 9, the first metal layer may be embodied by layer (212), which would allow the embodiment of a subsequent layer of metal between said first and second metal layers by layer (208).

As to claim 25, Huang et al., Figures 5A and 5B, discloses particular values for the width of the conducting pathways formed as vias, which would imply particular cross sectional areas of the vias.

As to claim 26, the extension line (212a) in Figure 4 may be of variable length, with larger resistance resulting from longer length and smaller resistance resulting from shorter length.

Claims 14-16, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al.. As to claim 14, Huang et al., Figures 3 and 4, discloses a pad area apparatus for a semiconductor structure comprising a substrate (150), a first layer of metal (208) disposed above said substrate, a second layer of metal (204) disposed over said first layer of metal, an electrostatic discharge protective device wherein said electrostatic discharge protective device is disposed within said substrate and wherein said electrostatic discharge protective device comprises a transistor (218) and a resistance, embodied as the conductive structure formed below the pad (200) and above the transistor (218), a layer of dielectric (230) disposed between said first metal layer and said second metal layer, and a via (202) disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer wherein said via comprises a plurality of individual vias and wherein said resistance comprises a portion of said plurality of individual vias wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

As to claim 15, Huang et al. discloses (col. 4, lines 35-39) that the conductive structure comprised of layers (204, 208, 212) and vias (202, 206, 210), as well as lines (226, 222, 212a) and (224, 220, 214) may all be formed from polysilicon, which has a known resistance. The fabrication of this structure determines the amount of polysilicon used, and therefore fixes the overall resistance.

As to claim 16, the structure of Huang et al., Figure 4, would have more resistance if fewer vias were formed, and less resistance if more vias were formed. See (col. 4, lines 45-50).

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As to claim 23, Huang et al., Figures 5A and 5B, discloses particular values for the width of the conducting pathways formed as vias, which would imply particular cross sectional areas of the vias.

As to claim 24, the extension line (212a) in Figure 4 may be of variable length, with larger resistance resulting from longer length and smaller resistance resulting from shorter length.

Claims 18-20, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al.. As to claim 18, Huang et al., Figures 3 and 4, discloses an electrostatic discharge protection device for a semiconductor structure comprising a resistance embodied as the conductive structure formed below the pad (200) and above the transistor (218) disposed within a substrate below a pad area (200) of said semiconductor structure wherein said resistance comprises a plurality of vias of said semiconductor structure, wherein said vias are arranged electrically in parallel, one to another.

As to claim 19, Huang et al. discloses (col. 4, lines 35-39) that the conductive structure comprised of layers (204, 208, 212) and vias (202, 206, 210), as well as lines (226, 222, 212a) and (224, 220, 214) may all be formed from polysilicon, which has a known resistance. The fabrication of this structure determines the amount of polysilicon used, and therefore fixes the overall resistance.

As to claim 20, the structure of Huang et al., Figure 4, would have more resistance if fewer vias were formed, and less resistance if more vias were formed. See (col. 4, lines 45-50).

As to claim 21, Huang et al., Figures 5A and 5B, discloses particular values for the width of the conducting pathways formed as vias, which would imply particular cross sectional areas of the vias.

As to claim 22, the extension line (212a) in Figure 4 may be of variable length, with larger resistance resulting from longer length and smaller resistance resulting from shorter length.

Claims 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al.. As to claim 27, Huang et al., Figures 3 and 4, discloses method of fabricating a semiconductor structure comprising disposing a pad area (200) upon a substrate (230), disposing an electrostatic discharge protective device disposed below said pad area, said electrostatic discharge protective device comprising a transistor (218) and a resistance, embodied as the conductive structure formed below the pad (200) and above the transistor (218), wherein said pad area comprises: a substrate (150), a first layer of metal (208) disposed above said substrate wherein said electrostatic discharge protective device is disposed

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below said first layer of metal, and a second layer of metal (204) disposed above said first layer of metal, disposing a layer of dielectric (230) disposed between said first metal layer and said second metal layer, and disposing a via (202) disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, and wherein said via comprises a plurality of individual vias and said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

As to claim 28, Huang et al. discloses (col. 4, lines 35-39) that the conductive structure comprised of layers (204, 208, 212) and vias (202, 206, 210), as well as lines (226, 222, 212a) and (224, 220, 214) may all be formed from polysilicon, which has a known resistance. The fabrication of this structure determines the amount of polysilicon used, and therefore fixes the overall resistance.

As to claim 29, Huang et al., Figures 5A and 5B, discloses particular values for the width of the conducting pathways formed as vias, which would imply particular cross sectional areas of the vias.

As to claim 30, the extension line (212a) in Figure 4 may be of variable length, with larger resistance resulting from longer length and smaller resistance resulting from shorter length.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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srw

January 13, 2005

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